MP0390

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. _____

Application No.:	10/626,507
Filing Date:	July 24, 2003
Appellants:	Son Ho et al.
Conf. No.:	1965
Group Art Unit:	2188
Examiner:	Kaushikkumar Patel
Title:	LINE CACHE CONTROLLER

REPLY BRIEF TO EXAMINER'S ANSWER

Mail Stop Appeal Brief-Patents
P.O. Box 1450
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November 16, 2008

Sir:

Pursuant to 37 CFR 1.193(b)(1), Appellant responds to the new points raised in the Examiner's Answer mailed September 16, 2008.

(1) REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in the Appeal Brief.

(2) RELATED APPEALS AND INTERFERENCES

A statement identifying the related appeals and interferences is contained in the Appeal Brief.

(3) STATUS OF THE CLAIMS

A statement identifying the status of the claims is contained in the Appeal Brief.

(4) STATUS OF AMENDMENTS

A statement identifying the status of amendments is contained in the Appeal Brief.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

A summary of the claimed subject matter is contained in the Appeal Brief.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in the Appeal Brief.

(7) RESPONSE TO EXAMINER'S ANSWER

Independent Claims 1, 12, 16, 19, 21, 44, 51, 55, 58, 59, 79, 90, 94, 96, and 98

With respect to claim 1, Appellants submit that Zaidi, either alone or in combination with any of the other cited prior art references, fails to show, teach, or suggest at least a switch including a plurality of selectors that each receives a second address and each selects between first and second sets of signals relating to first and second memory devices, respectively, based on the second address, and further submit that this structure is not inherent in the other cited prior art references.

As best understood by Appellants, Zaidi fails to disclose this limitation. Appellants respectfully note that the Examiner relies on a MAC 140 to disclose the claimed switch and the plurality of selectors. Here again, Appellants respectfully submit that the MAC 140 does not **necessarily** include a plurality of selectors as Appellants' claims recite. In fact, Appellant respectfully notes that the MAC 140 does not selectively receive data based on switching, and instead receives all data over a "shared memory bus" 104. The Examiner still fails to provide any reference to support an allegation that the MAC 140 includes structure analogous to the plurality of selectors as the claims recite.

Here again, the Examiner relies on the MAC 140 to disclose the switch. Consequently, the MAC 140 must also include **a plurality of selectors** that each receive the second address and select between sets of signals based on the second address. Neither Zaidi nor any other cited prior art reference appears to suggest that the MAC 140 would include such a structure.

Attempting to make up for the deficiencies of Zaidi, the Examiner further notes that Jeddeloh discloses that a switch 160 "can be a set of multiplexers," and relies on Jeddeloh to support the assertion that the plurality of selectors would be inherent in the MAC 140 of Zaidi. Initially, Appellants respectfully note that that the claims recite that the plurality of selectors **each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address**, and a mere reference to a set of multiplexers fails to disclose the specific

structure of this limitation. The Examiner provides no evidence that the switch 160 of Jeddeloh includes a plurality of selectors that select between sets of signals based on a second address (i.e. an address in a memory select portion of an address signal).

The Examiner now alleges that "Examiner never noted that the structure is inherent, but instead it is stated that 'selection of respective signals are inherent in the system of Zaidi' and the switch **can** include a plurality of selectors." (Emphasis added; see Page 4 of the Examiner's Answer mailed September 16, 2008). Appellant respectfully disagrees and submits that such reasoning still requires that the system of Zaidi **necessarily** includes a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address. In relying on an inherency argument, the Examiner must still establish that this structure is necessarily present in the MAC 140, and fails to do so.

Further, the Examiner alleges that "appellant is arguing the limitations that are not in the claims" because the claims do not recite how the switch is connected. See Pages 3-4 of the Examiner's Answer). Appellant respectfully disagrees. Here again, the MAC 140 views/receives all data packet traffic on a bus and directs the data packets according to address fields. Accordingly, the MAC 140 as described in Zaidi is not sometimes connected to one device and connected to another device at other times. Instead, the MAC 140 appears to be connected to both of the devices (e.g. flash 106 and SDRAM 108) at all times via the same interface (i.e. the **shared** bus 104). This structure is in complete contradiction to the structure of Appellants' claims, as well as the alleged "inherent" structure described in Jeddeloh. The relied upon limitation ("a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address") is directly contrary to a shared bus because the MAC 140 does not appear to select between sets of different signals on the shared bus based on a second address.

CONCLUSION

Neither Zaidi nor Jeddeloh discloses a switch including a plurality of selectors that each receives a second address and each selects between first and second sets of signals relating to first and second memory devices, respectively, based on the second address. Appellants, therefore, respectfully submit that the pending claims are not properly rejected under either 35 U.S.C. §103 and/or 35 U.S.C. §103 with an inherency argument.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Damian M. Aquino, Reg. No. 54,964, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By: 

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MDW/DMA/rao

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